Notched Spacer for CMOS Transistors

ABSTRACT OF THE DISCLOSURE

A notched spacer for CMOS transistors and a method of manufacture is provided. A gate electrode is formed on a substrate. A first ion implant mask is formed alongside the gate electrode such that the first ion implant mask is at least partially removed along the surface of the substrate. A first ion implant is performed at an oblique angle to the surface of the substrate to implant impurities of a first conductivity type in the substrate beneath at least a portion of the gate electrode. A second ion implant is performed at an angle normal to the surface of the substrate to implant impurities of a second conductivity type to form source/drain extensions of the CMOS transistors. Additional spacers and ion implants may be performed to fabricate graded source/drain regions.